4. The backup management system of claim 3, wherein the computer system includes at least one I/O card backplane and a system backplane, and said high-availability controller powers down the system sequentially, in the following order:

last logical said I/O card backplane, then associated said cell board;
highest logical said I/O card backplane, then associated said cell board; and
said system backplane.

5. The backup management system of claim 4, wherein, in response to detecting inactive processor status signals from all said management processors, if said high-availability controller detects that the power switch was pressed, said high-availability controller powers down the system sequentially.

6. The backup management system of claim 1, further including a power switch, for controlling bulk power to the computer system, coupled to said management processors and said high availability controller; wherein said high-availability controller is responsive to an output from the power switch to initiate powering down of each said power supply when the management processors have failed.

7. The backup management system of claim 1, wherein each of said management processors includes a watchdog timer that sets its said processor status signal to an inactive state when the respective management processor does not reset the timer within a predetermined period of time.

8. A method for multiple redundancy backup management of basic system functions in a computer system, the method comprising the steps of:

monitoring, via a plurality of management processors, a plurality of sensors for detecting power, temperature, and cooling fan speed in the computer system;

generating a plurality of processor status signals, each signal indicating an operational state of an associated one of said management processors;

monitoring said plurality of processor status signals; and

generating, in response to detecting that all of said processor status signals are inactive, backup control signals, in response to outputs from said sensors, to control operation of said controllers;

wherein said backup control signals are generated by a non-software coded state machine, operably coupled to said management processor, said sensors, and said controllers.

9. The method of claim 8, wherein said state machine performs a different sequence of operations than the code executed by said management processor.

10. The method of claim 8, wherein said sensors include at least one cooling fan controller for detecting and controlling said cooling fan speed, and a plurality of power controllers, each of which monitors the state of, and controls power to, an associated power supply in the computer system, including the step of:

sending said control signals and said backup control signals to said power controllers and to said fan module.

11. The method of claim 8, including the step of setting, for each of said management processors, a watchdog timer that generates an inactive said processor status signal for the associated one of said management processors when the management processor does not reset the timer within a predetermined period of time.

12. The method of claim 8, including the step of sequentially powering down the system in response to detecting inactive processor status signals from all said management processors, if a fan fault is detected or if a backplane power good signal is not detected.

13. The method of claim 12, wherein the computer system includes at least one I/O card backplane and a system backplane, and wherein the step of powering down the system sequentially comprises the following steps in the following order:

powering down the last logical said I/O card backplane, then associated said cell board; and

powering down the highest logical said I/O card backplane, then associated said cell board; and

powering down said system backplane.

14. The method of claim 13, wherein, in response to detecting inactive processor status signals from all said management processors, if said high-availability controller detects that the power switch was pressed, said high-availability controller powers down the system sequentially.

15. A backup management system for providing basic system control functions in a computer system comprising:

a plurality of system sensors for detecting signals from at least two devices in the group of devices consisting of a power module for monitoring the state of an associated power supply in the computer system, a temperature sensor for monitoring temperature in the computer system, and a cooling fan speed module for detecting and controlling system cooling fan speed;

a plurality of management processors, wherein each of the processors is coupled to each of said sensors;

wherein a management processor status signal is generated by each of said management processors to indicate an operational state thereof;

a non-software coded state machine, operably coupled to each of said management processors and to said system sensors, wherein said state machine performs a different sequence of operations than the code executed by said management processors;

wherein, in response to detecting that each said status signal is inactive, said state machine generates control signals to said power controllers and to said fan module in response to outputs from said system sensors to control the operation thereof.

16. The backup management system of claim 15, wherein said controllers include:

a plurality of power controllers, each of which monitors the state of an associated power supply in the computer system, and controls power thereto; and

at least one cooling fan controller for detecting and controlling said cooling fan speed.

17. The backup management system of claim 15, wherein each said management processor includes a watchdog timer that sets said processor status signal for the associated processor to an inactive state when the management processor does not reset the timer within a predetermined period of time.

18. The backup management system of claim 15, wherein, in response to detecting inactive processor status signals from all said management processors, if a fan fault is detected or if a backplane power good signal is not detected, said high-availability controller sequentially powers down the system.

19. The backup management system of claim 18, wherein the computer system includes at least one I/O card backplane and a system backplane, and said high-availability controller powers down the system sequentially, in the following order:

last logical said I/O card backplane, then associated said cell board;
highest logical said I/O card backplane, then associated said cell board; and
said system backplane.

20. The backup management system of claim 19, wherein, in response to detecting inactive processor status signals from all said management processors, if said high-availability controller detects that the power switch was pressed, said high-availability controller powers down the system sequentially.